REMARKS

The examiner has rejected claims 1-3 under 35 USC 102 (b) as anticipated by Jeddeloh, U.S. Patent 5,935,233. The examiner also rejected claims 1, 4, and 9 under 35 U.S.C. 102 (e) as anticipated by Pawlowski, U.S. Patent 6,401,153.

The Examiner has rejected claims 5, 6, 10, and 11 under 35 U.S.C. 103 as obvious over Pawlowski in view of Jeddeloh, specifically referencing "columns 46-48". The Examiner also rejected claims 7 and 8 over Pawlowski in view of Jeddeloh and further in view of Neal, U.S. Patent 5761462.

The Examiner has rejected claim 17 over Pawlowski in view of Jeddeloh, in further view of *Reconfigurable computing: What, why, and Implications for Design Automation* by DeHon.

In his application of Jeddeloh to the claims, the Examiner makes frequent reference to "columns 46-48". It should be noted that Applicant finds no column numbered higher than 18 in U.S. patent 5,935,233 to Jeddeloh. Similarly, Pawlowski and Neal both end with column 10. Applicant is therefore uncertain of the material the examiner intended to cite.

New Claims

New claim 18 corresponds in scope approximately to original claim 2, with the limitations of original claims 7 and 8, and incorporates the substance of original parent claim 1. New claim 19-20 incorporate elements of implementation in an FPGA, auto- programmability, and FIFO bypass feature not having exact parallels in the old claims.

New claim 21 extends claim 17 by adding the FIFO bypass feature of Claim 13.

Amended Claims

The claims have been amended in accordance with the Examiner's helpful suggestions. In addition to these amendments, several claims have been cancelled and the scope of the claims limited to bus bridges having JTAG busses as target busses.

Jeddeloh, Pawlowski, and Claims 1-4 (now part of Claim 18) and Claim 9

Jeddeloh, U.S. Patent 5,935,233, describes a PCI bus bridge. This device passes bus transactions from a first PCI bus onto a second PCI bus. PCI buses, such as the first and second PCI busses of Jeddeloh, however, are not a *serial* bus as claimed; PCI busses are generally considered parallel busses.

In the art, the term "serial bus" is generally understood to refer to a bus having zero or more clock and control lines, and a single data line. Such busses are generally capable of transmitting only one "bit" of information per reference edge of a clock signal; both the JTAG and IIC busses discussed in the present application are serial busses according to this definition.

The PCI bus has a plurality of data lines, in some implementations 32 data lines and in others 64 data lines. The PCI bus has clock lines and control lines such that it is generally capable of transmitting from 8 to 32 or 64 bits of information in a clock cycle. The PCI bus is therefore generally considered to be a parallel bus and not a serial bus.

Pawlowski Figure 2 as cited by the examiner illustrates a serial bus controller device capable of interfacing a processor bus to a serial bus. The processor bus of Pawlowski is specifically referenced as a parallel bus at line 57, column 2.

Since neither Jeddeloh nor Pawlowski fails to provide every element of the claim, rejection under 35 U.S.C. 102 (b) or (e) of claims 1-4 and 9 is improper.

35 U.S.C. 103 Rejections

The Examiner has relied on Jeddeloh for many key elements of all 35 U.S.C rejections in this action. Such a key element is the idea of a bridge from a first serial bus to a second serial bus. Jeddeloh, however, describes a parallel bus and therefore fails to provide this element. While the serial port interface of Pawlowski can also be described as a bus bridge, as described in Pawlowski this acts between a parallel bus and a single serial bus.

The Examiner relies on Pawlowski for apparatus, controllable over a bus, for selecting between multiple serial ports. Pawlowski fails to provide multiple serial ports, the additional ports could be ports of other types.

It is known in the art that parallel and serial busses often pose different requirements. For example, parallel busses are generally accompanied by clock lines bearing continuous clock signals, where each line is sampled at only one edge of a clock, while serial busses pose issues of clock recovery and may require sampling the same line on both edges of a clock. For these, and other reasons, including the generally lower expected performance of serial busses, designers of serial to serial bus bridges tend not to rely much on the art of parallel to parallel bus bridges.

Claims 17 and 19-21 require that the bus bridge be implemented in an FPGA, that configuration code for the FPGA be in an EEPROM, and that the EEPROM be erasable and writeable through the bus bridge. Some of these claims also have the additional limitation of a bypass mode whereby the EEPROM containing configuration code for the bus bridge can be written without using portions, such as FIFOs in the bus bridge.

The Examiner has relied on DeHon for the element of an EEPROM coupled to provide configuration code for an FPGA, the FPGA then implementing the bus bridge.

It is well recognized that firmware of computer systems, including FPGA code in computer systems, may have errors requiring replacement of the code. Applicant admits that using an EEPROM to contain configuration code for an FPGA, as described in DeHon, is common in the art of reconfigurable logic.

Nowhere in the cited art, however, is it suggested that a bus bridge be used to reprogram the FPGA code with which it is implemented, and thereby be capable of being used to *reconfigure itself.* Indeed, many designers would shy away from this implementation, because if any error occurs in programming that EEPROM containing the bus bridge FPGA code, the system could be effectively locked into a defective state--since that EEPROM as well as any others accessed through the bridge may no longer be accessible.

Applicant believes that the bypass mechanism claimed provides advantage in that, should the EEPROM be provided with erroneous code such that major portions (such as but not necessarily limited to the FIFOs) of the bridge be rendered inoperable, the system can be recovered by using the bypass mode for programming the EEPROM.

The bypass mode also does not appear anywhere in the cited art.

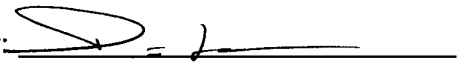
CONCLUSION

Applicant submits that the original 35 U.S.C. 102 rejections were improper, and that the 35 U.S.C rejections have been overcome. Applicant therefore respectfully requests that the Examiner reconsider the application as hereby amended.

Pursuant to 37 CFR 1.17, the $110.00 fee for the extension of time should be applied against our Deposit Account No. 12-0600. Applicant believes no fees are currently due, however, if any fee is deemed necessary in connection with this Amendment and Response, please charge Deposit Account No. 08-2025.

Respectfully submitted,

LATHROP & GAGE L.C.

By: 

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